

Dr. Gayles also managed the CPU in Intel’s first productized IA SOC – targeted for digital home and connected computing applications. Additionally he managed Intel’s first PCH silicon design and proposed the first architecture for Phase-Change Memory / IA CPU integration. Dr. Gayles research leadership led to the formation of Intel’s first industry recognized Cloud Computing initiative, new University research programs based on Massively Parallel IA, and the formation of a new Wireless Health research center.

Dr. Gayles’ key research areas include low power, VLSI circuit architectures, advanced I/O, and packaging. He successfully applied his expertise during his tenure in Intel – having received a significant number of corporate awards and recognitions for advancing the quality and performance of Intel’s processors. He also has an extensive software background and has managed CAD organizations responsible for CPU timing, and reliability.

Having held senior leadership positions over 16 years on a vast number of Intel Microprocessor products, Dr. Gayles has demonstrated unquestioned leadership abilities managing some of the most complex high tech projects developed in recent years. Throughout his tenure as a Director within Intel Research, Dr. Gayles confirmed his extensive expertise directing high value, advanced strategic research initiatives.

Research programs under Dr. Gayles’ guidance included Cloud Computing, Graphics, and advanced system memory architectures. He holds several patents in the field and has published numerous papers. Dr. Gayles earned degrees in Computer Science and Engineering from the University of Maryland Baltimore County and Pennsylvania State University. He is also fluent in Spanish.

Dr. Gayles’ leadership in microprocessor design, high tech program management, and advanced research spans 17 years. He has managed engineering teams in the U.S., Latin America, and Asia. He is currently Technical Director and Solutions Architect for Intrinsix – serving as the Engineering Manager for California. Previously he served as a Director within Intel Research and as a Senior Engineering Project Manager. His programs and technical innovations have led to the productization of significant technologies in the areas of Low Power Electronics, High Speed I/Os, Connected Computing, and advanced Memory Systems.

Dr. Gayles managed the Circuits Lab of the Low Power Research Group in the late 90’s. This was Intel’s first low power research activity covering circuits – which led to a 30% reduction in power across IA CPUs. He subsequently managed several CPU teams whose accomplishments included the first on-die L2 Cache integration for an IA processor, the first Integrated Back-Side Bus architecture, the first High Speed, 4-Way FSB architecture for servers, and Intel’s first C4 IA processor. Dr. Gayles innovated the technology and built a team specifically for IA CPU power analysis. This team’s key accomplishment was the development of a new algorithm implementing a gate level fine grained power analysis tool which consistently predicted power across four process generations to within 3% - being code set specific. This was a first for Intel.

Dr. Gayles led several startup, acquisition, and investment evaluations across multiple business groups during his tenure at Intel. A technology sampling includes:

* Reconfigurable computing
* Low Power RTL Synthesis
* Rapid SOC synth. & IP integration
* Cloud Computing
* RF subsystem partitioning
* BIO + ULSI system integration

***Technical Director and Solutions Architect***

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**Career Synopsis**

*- Microprocessor Design*

*- ASICs and SOCs*

*- Project Management*

*- VLSI IC and System Design Consulting*

*- Startup & M/A Evaluations*

*- Advanced Research*

**Technical Coverage**

*- IC Design*

*- SOC/POC*

*- Energy Efficient Systems*

*- Advanced Packaging & IO*

*- Reconfigurable Computing*

*- Novel Memory Technologies*

*- Mixed-Signal Systems*

**Ph.D. Computer Science and Engineering:**Pennsylvania State University. 1992 – 1996.

*Thesis Title: Building High Speed, Energy Efficient CMOS Circuits Using Variations in Circuit Techniques*

**EXECUTIVE PROFILE**

Eric Gayles, Ph.D.

### Doc GreenRESUME – Page 1 Eric Gayles, Ph.D.

**Executive Electronics/ IT/Design Engineering Management**

Program/Product Design Leadership │ Advanced Research │ Global Team Development

* Experienced and award winning **executive engineering management leader** with a track record of managing projects with exceptional success and working across multi-disciplinary global teams to deliver results in engineering that are innovative and lead to successful project deliverable outcomes.
* Career focus on integrating sound knowledge of electronic engineering, design and development principles.
* A track record of consistently anticipating consequences of new designs, initiating solutions and completing projects to specification.
* Engineering experience includes design/development of manufacturing processes, testing and quality control.
* Accomplishments include design and development of sophisticated silicon/microprocessor products and the advancement of high-performance technical projects.

**Core Competencies**

* Microprocessor Design Mgmt
* Building and leading successful international organizations
* Development of new silicon technologies
* Analog, Clock, and I/O
* IC packaging
* Envr. sensitive design
* Low Power Circuit innovator
* Program / Project Management
* Strategic Planning
* SOC design and management
* Tech Startup and M&A
* Leading Advanced Research

- Product Development

**Professional Experience**

**Selected Accomplishments**

**High Performance Microprocessors:** Over 10 tapeouts of performance leading products in high volume end to end deployment

**Microprocessor Design Manager**: Intel’s first IA System on a Chip – Digital Home. First PCH (Next gen Southbridge) for CPU+Graphics

**Next Generation Memory Architecture**: Memory and Storage Architecture for Phase Change Memory in Low Power, High Performance IA Computing. $1B in BOM savings and 30% in projected power reduction over the next decade.

**Analog, Mixed Signal Leader**: Intel’s 1st High Speed, 4-Way FSB architecture for servers and Intel's 1st C4 IA processor

**Low Power Lab Research Manager**: Circuit innovations & BKMs lowered power consumption 30% across CPU designs. Innovated a CAD suite predicting chip power per application to within 3% of actual. Design Automation Manager for Intel’s 7GHz processor program

**Technical Strategy**: Served as driving force behind the Intel's 1st industry recognized Open Source Cloud Computing initiative, the creation/launch of a new Wireless Health Research Center, and implemented new university research programs on Massively Parallel IA

**Intrinsix Corporation**

**2013 to Present: Engineering Director and Solutions Architect**

* Provides technical leadership on customer projects.
* Technology development in analyzing customer requirements, architecting and proposing solutions.
* Crafts state-of-the-art solutions for complex Mixed-Signal design problems.
* Manages ASIC and SOC engineering design resources.

**Siquance Consulting**

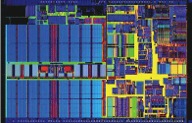
**2012: Director – Technical Lead Tech / Sr. Consultant & Project Manager**

Identified next generation game-changing R&D high-risk/high-payoff technology opportunities andoversaw ASIC development for Consumer Electronic Tablet Platforms and Startups.

**Intel Corporation, Santa Clara, CA**

**2008 to 2012: Director, External Programs & Senior Technologist / Research**

Managed the global effort for SOC Division around next generation memory architectures and Intel Lab’s program to influence the academic research agenda at the world’s leading universities. Key research programs included Wireless/Digital design initiatives in Healthcare, IA based high-end graphics, low power embedded systems, development of new Parallel Programming models for IA processors, and Cloud Computing.

* Oversaw Memory and Communications technical exploration for future Ultrabook and Tablet platforms
* Architected an innovative Memory and Storage Architecture for Phase Change Memory in Low Power, High Performance IA Computing, resulting in a 30% power reduction and $1B+ projection in savings for ultra mobility devices over the next decade
* Envisioned and directed the restructuring of Intel’s research partnership strategy with the world’s top universities to drive greater product line innovations, with a budget of $50M

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**RESUME** – Page 2 **Eric Gayles, Ph.D.**

**2007: Processor Design Manager: South Bridge Processor**

Oversaw all design processes and a $40M budget for the design & development of the 65nm Southbridge. Managed a team of 100 globally located designers that successfully developed a product capable of providing greater storage capabilities, integrated graphics, and enabled systems to perform significantly faster with low power/cost.

* Successfully deployed the (PCH) Peripheral Control Hub processor on schedule that allowed the transition from CPU to GPU+CPU integrated platforms and successful tape-out of the predecessor ICH10 processor.

**2006 to 2007:** **Program Manager: Digital Home Next Generation SOC Program**

Directed and led Intel’s Digital Home System on a Chip platform program for “Intelligent” TVs and targeting the broader market for home entertainment devices. Successfully managed the CPU, software, and firmware, and networking components with initial industry design wins of $500M in product profits and projected future generation profit success forecasted at more than $2B.

* Increased responsibility owning several high impact transformative Consumer Electronic programs
* Effective communications with CEO & Exec staff led to approval for development of a series of uniquely designed CPUs for SOCs across 3 process nodes and received approval for acquisition of a targeted silicon design startup.
* Led research on external joint ventures and business alliances for next generation display processing technologies and IP management tools.

**2004 to 2006: System on a Chip Engineering Design Manager and Program Manager: Vermilion Program**

Managed complete project deliverables for production of Intel’s first system on a chip for the digital television market. Oversaw complex collaborative processes covering multisite/international engineering team management, hardware/software co-design, Fab/process enhancements, and global software engineering. Successfully developed the design, manufacturing and testing of the SOC and the customer reference boards.

* Responsible for the leadership of 5+ product teams totaling 100-500 designers at 6 global sites in the USA (California/Arizona), the Middle East (Israel) and Asia (Malaysia)
* Productized all designs on schedule earning the company billions of dollars in revenue and setting the basis for several generations of future products on multiple roadmaps
* Managed the CPU Engineering and Productized Intel’s 1st IA SOC

**1998 to 2003: Circuit Design Manager: Desktop Products Group**

Demonstrated leadership and senior staff engineering management for Intel’s Desktop Product Group that served as the primary revenue source for Intel with billions of dollars in annual profit and product margins of well over 60%. Managed up to 25 circuit design engineers, 50 mask designers and 30 design automation engineers completing all product deliverables, while meeting all product/project milestones ahead of schedule.

* Acknowledged with numerous department and division level awards and promoted 3 times within 6 years in recognition of team leadership and project/product success.
* 1st On-die L2 Cache Integration for an IA Processor , 1st  Integrated Back-Side Bus Architecture
* 1st  High Speed, 4-Way FSB Architecture for Servers
* Intel's 1st C4 IA Processor

**1996 to 1998:** **Manager: Low Power Research Group**

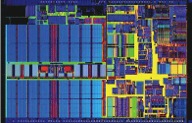
Recruited out of college to provide key research in low power electronic power design leadership and manage the newly formed low power research group. Assessed the power impact of Intel’s current circuit designs across various projects and focused on high ROI change methods, while developing new circuit topologies, and deploying new high impact BKMs across all revenue generating programs.

**Education**

Pennsylvania State University, University Park, PA

**Ph.D. Computer Science and Engineering**

Thesis Title: *Building High Speed, Energy Efficient CMOS Circuits Using Variations in Circuit Techniques*

University Of Maryland, Baltimore County, Baltimore, MD

**B.S**. **Computer Science** **with Honors**

***Foreign Language: Fluent in Spanish***

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**RESUME** – Page 3  **Eric S. Gayles, Ph.D.**

**Selected Publications**

1. E. Gayles, R.M. Owens, and M.J. Irwin, ``The MGAP-2: A Micro-Grained Massively Parallel Array Processor,'' Proceedings of Application Specific Integrated Circuits Conference, Sept, 1995, pp.333-337.
2. T. Kelliher, E. Gayles, R.M. Owens, and M.J. Irwin, ``The MGAP-2: An Advanced, Massively Parallel VLSI Signal Processor,'' Proceedings of the International Conference on Acoustics, Speech, and Signal Processing, 1995, pp. 3219-3222.
3. E. Gayles, R.M. Owens, and M.J. Irwin, ``A Fast Compact Addition Architecture for Low Power Microprocessors and DSP Chips,'' Proceedings of Application Specific Integrated Circuits Conference, 1996.
4. E. Gayles, R.M. Owens, and M.J. Irwin, ``Low Power Circuit Techniques for Fast Carry-Skip Adders,'' Proceedings of the Midwest Symposium on Circuits and Systems, 1996.
5. T. Kelliher, B. J. Bishop, Y. Zhang, E. S. Gayles, R. M. Owens, M. J. Irwin, ``The MGAP-2: Demonstration of a Massively Parallel Micro-Grained Array Processor,'' Proceedings of Supercomputing, Nov. 1996.
6. E. Gayles, K. Acken, R.M. Owens, M.J. Irwin, ``A Clocked, Static Circuit Technique for Building Efficient High Frequency Pipelines,'' Proceedings of The Seventh Great Lakes Symposium on VLSI, March 1997.
7. K. Acken, E. Gayles, T. Kelliher, R.M. Owens, M.J. Irwin, ``The MGAP Family of Processor Arrays,'' Proceedings of The Seventh Great Lakes Symposium on VLSI, March 1997.
8. E. Gayles, T. Kelliher, R.M. Owens, and M.J. Irwin, "The Design of the MGAP-2: A Mirco-grained Massively Parallel Array" to appear in Dec 2000, Vol 8, No 6, IEEE Transactions on VLSI Systems.
9. G. Taylor, J. Jones, J. Price, C.H. Lim, P. Newman, S. Mandal, M. Jahan, E. Gayles, "Overview of Coppermine/Cascades FSB Performance Enhancements, " Intel DTTC 1999.
10. E. Gayles, D. Covell, H. Oie, "PEACH - A New Power Grid Validation Tool for High Performance Microprocessors," Intel DTTC 2000.
11. Tensay Woldeyes , Mirza Jahan, Eric Gayles, Randy Jenkins, Keith MacPherson, “The Cascades 2M Microprocessor Package Design,” Intel Assembly Test and Technology Journal, 2000.

**Patents**

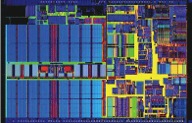
1. DATA ENABLED LOGIC CIRCUITS - U.S. Patent awarded- 6/17/2000 (Patent # 6,078,196)
2. FAST-SWITCHING LOGIC GATE - U.S. Patent awarded - 11/2/1999 (Patent # 5,977,789)
3. A CONTENTION-FREE, LOW CLOCK LOAD DOMINO CIRCUIT TOPOLOGY - U.S. Patent awarded - 7/23/1999 (Patent # 6,191,618)
4. PRE-ANNOUNCE SIGNALING FOR INTERCONNECT BUILT-IN SELF TEST U.S. Patent pending - 3/31/2003
5. PUSH BUTTON MODE AUTOMATIC PATTERN SWITCHING FOR INTERCONNECT BUILT-IN SELF TEST – U.S. Patent Awarded – 11/30/2004 (Patent # 6,826,100)
6. AUTOMATIC SELF TEST OF AN INTEGRATED CIRCUIT COMPONENT VIA AC I/O LOOPBACK – U.S. Patent Awarded – 1/21/2006 (Patent # 7,139,957)

**Design**

Microprocessor Tape Outs:

* Pentium III – The original (Katmai) – I/O & Power Design Team Manager
* Pentium III XEON – 2M 180nm – (Cascades) – I/O, Power, and Estimation Design Team Manager
* Pentium III – Compaction to 180nm (Coppermine) – I/O, Power, and Estimation Design Team Manager
* Pentium III – 130nm (Tualatin) – Bus and Instruction Cluster Design team manager, I/O & Power Team Manger, Tapeout owner, Horizontal Design Methodologies Team owner
* Pentium V – 90nm (Tejas) – Horizontal Custom Digital Fubs owner, I/O Team Manager, Clock Team Manager, Project DA Manager

**Teaching Experience**

* Q1 1998: Course Developer and Instructor for Intel's Advanced Circuit Design Curriculum: *Low Power Circuit Design* Component
* Spring 1996: *Introduction to VLSI* Instructor for Stanford’s Splash Program
* Fall 1995: PSU Instructor of *Computer Science and Engineering 201* - *C programming*
* *for Engineers*
* Summers 1994 and 1995: Computer Science Instructor for the PSU sponsored *B.E.S.T Summer* *Program* for advanced high school students.
* ****Fall 1994 and Spring 1995: PSU Teaching Assistant for *Computer Science and Engineering*

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*203 - Computer* *Applications for Business Majors*